FPGA Based Reactor Protection System Architecture

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Outline

• Reactor Protection System (RPS) Introduction
• FPGA Introduction
• Background of FPGA based RPS
• CNEA I&C RPS Architecture
• Diverse FPGA Implementation
• Conclusions
Reactor Protection System Introduction

Reactor Protection System’s (RPS) primary goal -> fulfillment of the safety functions of a nuclear reactor:

- Reactivity Control
- Core Cooling
- Radionuclide contention

- Monitors the evolution of variables and detects deviations beyond safe limits
- Implements the protection logic which automatically demand the actuation of front safety systems
Reactors Protection System Introduction

• RPS functions are classified as “Category A” as defined in IEC 61226

• Design criteria:
  – Redundancy
  – Fail-safe
  – Single failure criterion
  – Design simplicity
  – Well known technology
  – Separation
  – Independence
  – Diversity
FPGA Based Reactor Protection System Architecture

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FPGA Introduction

FPGA: Field-programmable gate array

- Logic blocks implement combinational and sequential logic
- Routing resources to interconnect inputs, outputs and logic blocks
- I/O blocks to provide external connections to the chip

FPGA chip basic scheme
FPGA Introduction

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## FPGA Introduction

### Microprocessors (Software) vs FPGA

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<td>Short product life cycles</td>
<td>Long term support</td>
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- **Time consuming and expensive V&V process**
- **More attainable and affordable V&V process**
Background of FPGA based RPS

• FPGA advantages for RPS implementation
  – High reliability (As keep simple using only Finite State Machines and Combinational Logic)
  – Parallel nature
  – Portability using Hardware Description Languages (HDL)
  – Long term support

• IEC 62566 standard
  – IEC 62566 – Nuclear power plants – Instrumentation and control important to safety – Development of HDL – programmed integrated circuits for systems performing category A functions
  – The design process follows a Verification and Validation process similar to software V&V process.
Background of FPGA based RPS

- Requirements Specification
- Verification
- Design
- Verification
- Implementation
- Verification
- System Integration
- Verification
- System Validation

IEC 62566 standard
Background of FPGA based RPS

• CNEA I&C previous experience:
  – 2002: SCRAM Logic for RA-1 Research Reactor (CPLD Based Module)
  – 2012: Alternative Instrumentation for Atucha II NPP Boron Injection Safety System (Similar architecture to current project for RA10 and CAREM RPS)

• Other implementations examples:
  – Radiy (Ukrainian)
  – Lungmen (Taiwan)
  – Rolls-Royce (UK)
  – Toshiba (Japan)
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Background of FPGA based RPS
SCRAM Logic for RA-1 Research Reactor (2002)
Background of FPGA based RPS

Alternative Instrumentation for Atucha II NPP Boron Injection Safety System (2012)
CNEA I&C RPS Architecture
Triple Redundancy Architecture for RA10
Diverse FPGA Implementation

The Common Cause Failure (CCF) is an important issue in safety systems based on software and FPGA technology. It is known that the implementation of diversity reduces the probability of CCF occurrences (IEC 61508 Part 7 Section B.1.4 [12]).
Diverse FPGA Implementation

Diversification styles in CNEA I&C RPS:

- Developers team
- FPGA Manufacture & Technology
- PCB Board Technology
- Most of other components
Diverse FPGA Implementation

• Each pair of modules work in parallel in the same train
• There is no priority between diversities
• Real time cross-verification between diverse modules

Eg.

Comparators Diversity A

Real-time cross-verification

Comparators Diversity B
Diverse FPGA Implementation
Train Diagram Block

FPGA Based Reactor Protection System Architecture
Diverse FPGA Implementation
Diverse FPGA Implementation
Conclusions

• The use of FPGA technology, as the main component of RPS design, has proven to be very effective.
• The goal of a simple design was achieved by using FPGAs, finite states machines and one-way communication channels.
• CCF issue is addressed using diverse FPGA implementation running in parallel in each train.
• The requirements for independence, isolation and wiring complexity reduction are fulfilled using serial transceivers over optical fiber.
Questions

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